Lecture 07
DC and AC Load Line

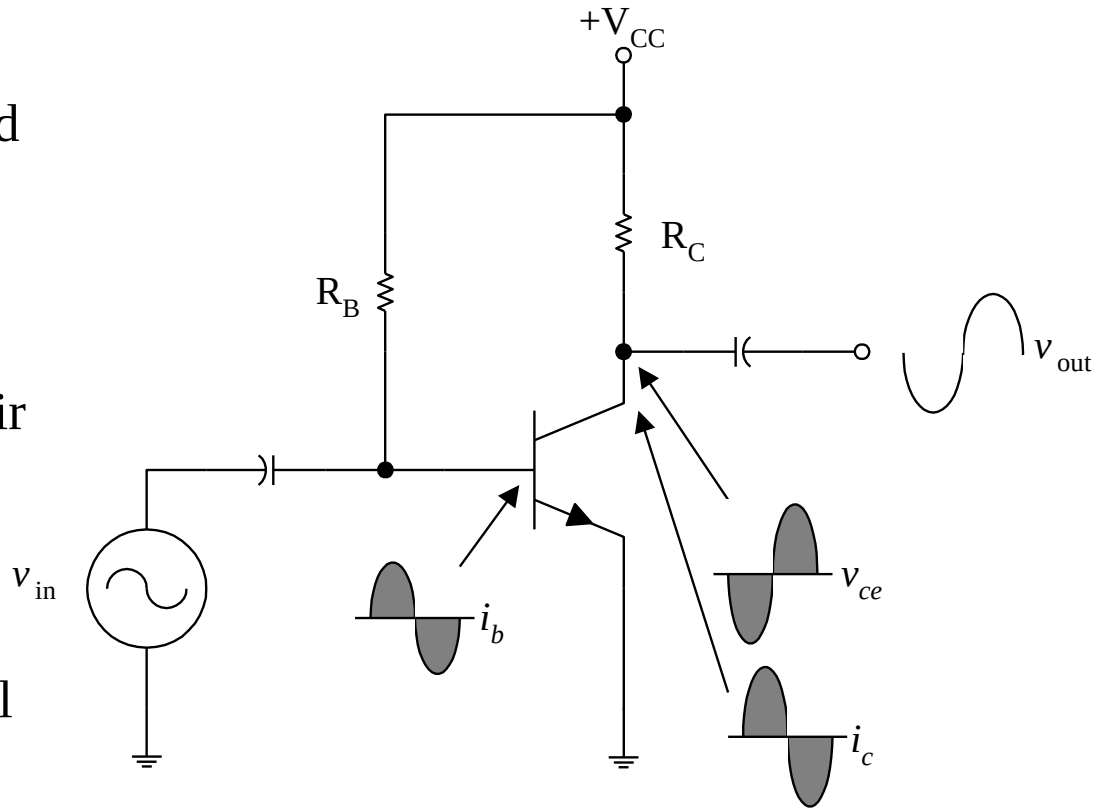
- DC biasing circuits
- DC and AC equivalent circuit
- Q-point (Static operation point)
- DC and AC load line
- Saturation Cutoff Condition
- Compliance

Book Reference

- Electronic Devices and Circuit Theory by Robert Boylestad & Louis Nashelsky (Prentice Hall)
- Electronic Devices by Thomas L. Floyd (Prentice Hall)

DC Biasing Circuits

- The **ac** operation of an amplifier depends on the initial **dc** values of I_B, I_C, and V_{CE}.
- By varying I_B around an initial dc value, I_C and V_{CE} are made to vary around their initial dc values.
- **DC** biasing is a static operation since it deals with setting a **fixed (steady)** level of current (through the device) with a desired fixed voltage drop across the device.



Purpose of the DC biasing circuit

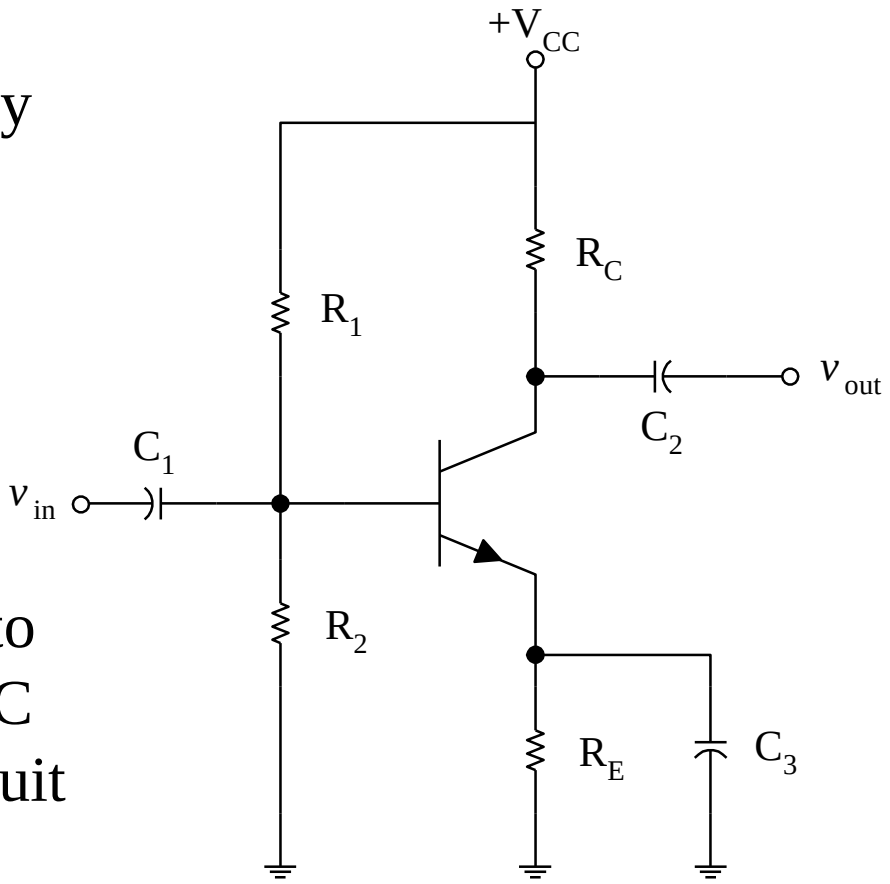
- To turn the device “ON”
- To place it in operation in the region of its characteristic where the device operates most linearly, i.e. to set up the initial dc values of I_B, I_C, and V_{CE}

Voltage-Divider Bias

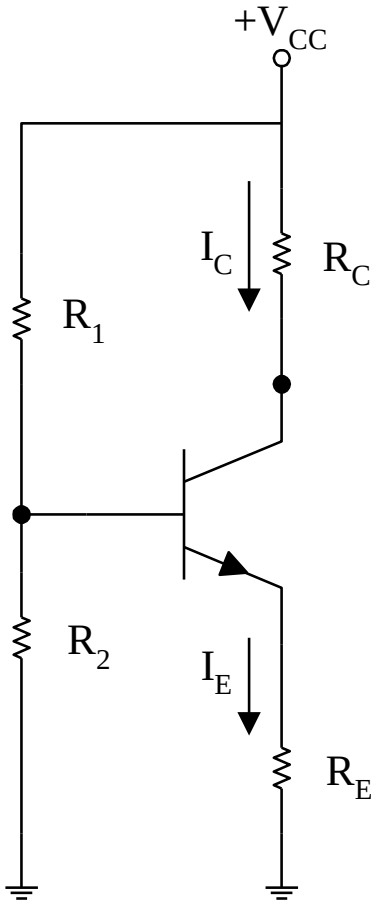
- The voltage – divider (or potentiometer) bias circuit is by far the most commonly used.
- R_{B1}, R_{B2}
  $\Rightarrow$ voltage-divider to set the value of V_B , I_B
- C_3
  $\Rightarrow$ to **short circuit ac** signals to ground, while not effect the DC operating (or biasing) of a circuit

($R_E \Rightarrow$ stabilizes the ac signals)

$\rightarrow$ **Bypass Capacitor**



Graphical DC Bias Analysis



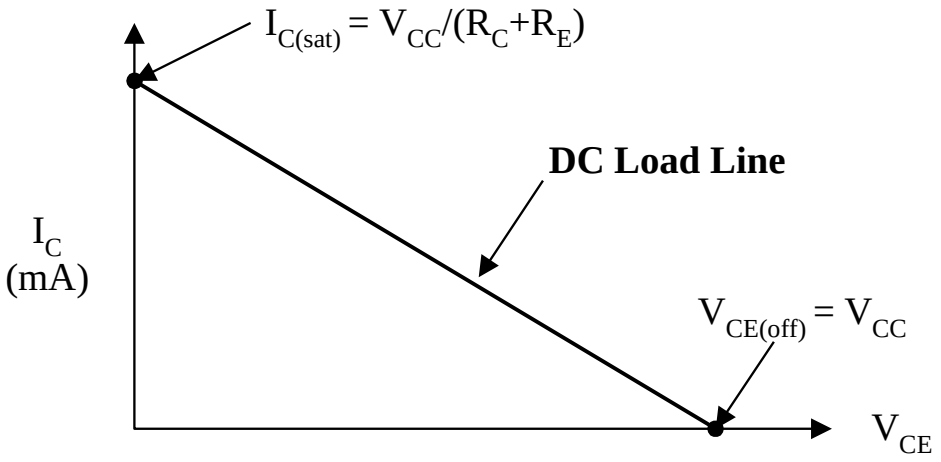
$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

for $I_C \approx I_E$

$$I_C = \frac{-1}{R_C + R_E} V_{CE} + \frac{V_{CC}}{R_C + R_E}$$

Point - slope form of straight line equation :

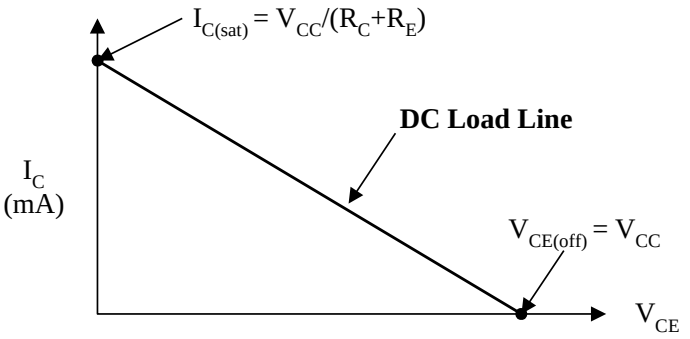
$$y = mx + c$$



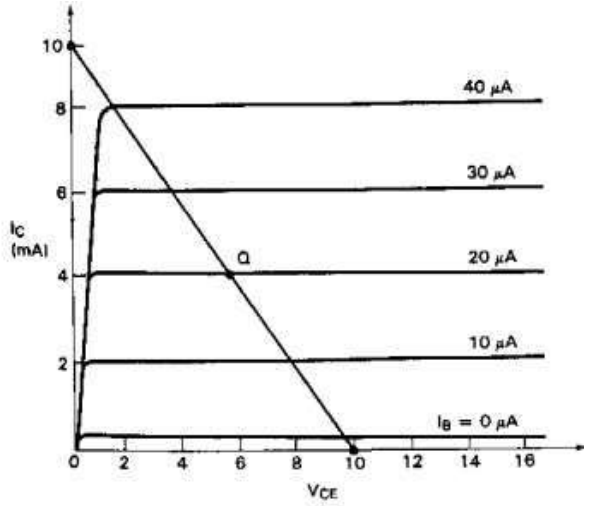
DC Load Line

•The straight line is know as the **DC load line**

•Its significance is that regardless of the behavior of the transistor, the collector current I_C and the collector-emitter voltage V_{CE} must always lie on the load line, depends ONLY on the V_{CC}, R_C and R_E



•(i.e. The dc load line is a graph that **represents all the possible combinations of I_C and V_{CE} for a given amplifier**. For every possible value of I_C, and amplifier will have a corresponding value of V_{CE}.)



•It must be true at the same time as the transistor characteristic. Solve two condition using simultaneous equation

What is $I_{C(sat)}$ and $V_{CE(off)}$?

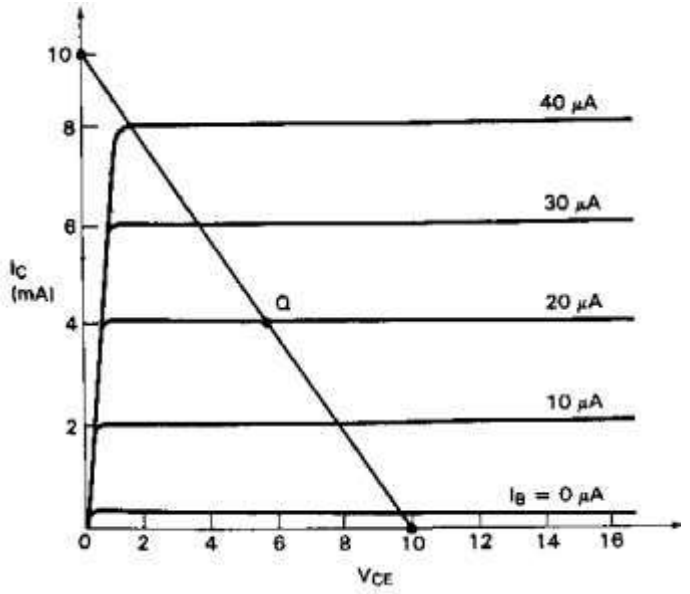
$\rightarrow$ graphically $\rightarrow$ **Q-point !!**

Q-Point (Static Operation Point)

- When a transistor does not have an **ac input**, it will have **specific dc values** of I_C and V_{CE}.
- These values correspond to a specific point on the **dc load line**. This point is called the ***Q-point***.
- The letter ***Q*** corresponds to the word (Latent) **quiescent**, meaning **at rest**.
- A quiescent amplifier is one that has no ac signal applied and therefore has constant dc values of I_C and V_{CE}.

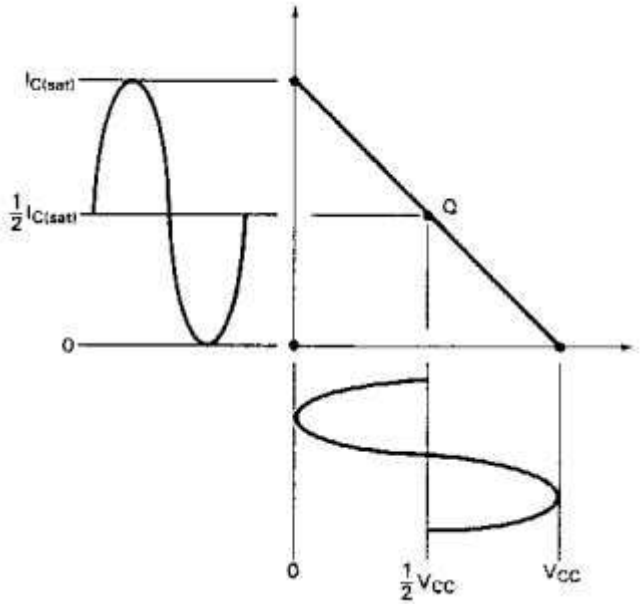
Q-Point (Static Operation Point)

- The intersection of the dc bias value of I_B with the dc load line determines the *Q*-point.
- It is desirable to have the *Q*-point centered on the load line. Why?
- When a circuit is designed to have a centered *Q*-point, the amplifier is said to be midpoint biased.
- Midpoint biasing allows optimum ac operation of the amplifier.

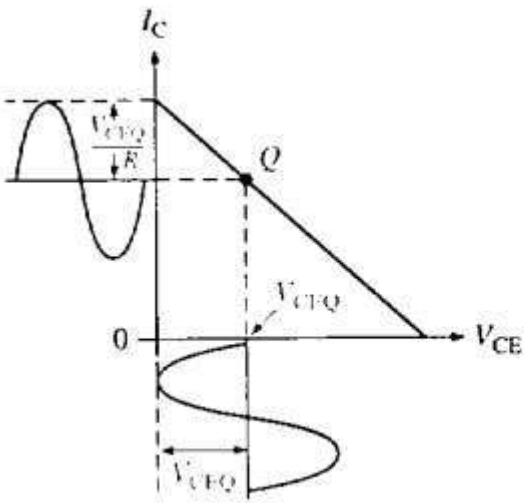


DC Biasing + AC signal

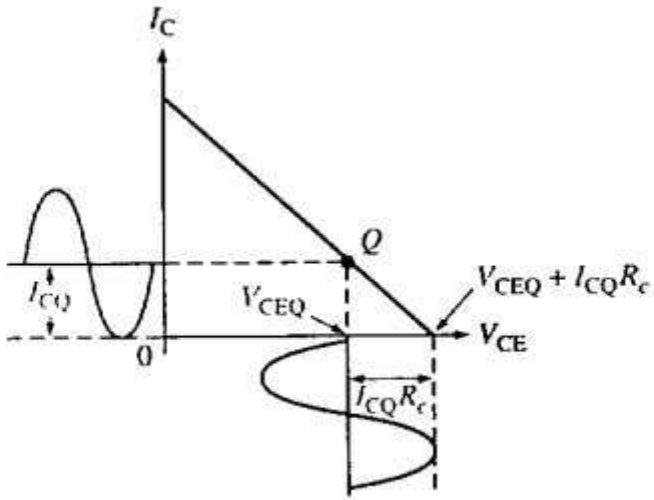
- When an **ac signal** is applied to the base of the transistor, I_C and V_{CE} will both vary around their *Q*-point values.
- When the *Q*-point is **centered**, I_C and V_{CE} can both make the **maximum** possible transitions above and below their initial dc values.
- When the *Q*-point is **above** the center on the load line, the input signal may cause the transistor to saturate. When this happens, a part of the output signal will be ***clipped*** off.
- When the *Q*-point is **below** midpoint on the load line, the input signal may cause the transistor to cutoff. This can also cause a portion of the output signal to be clipped.



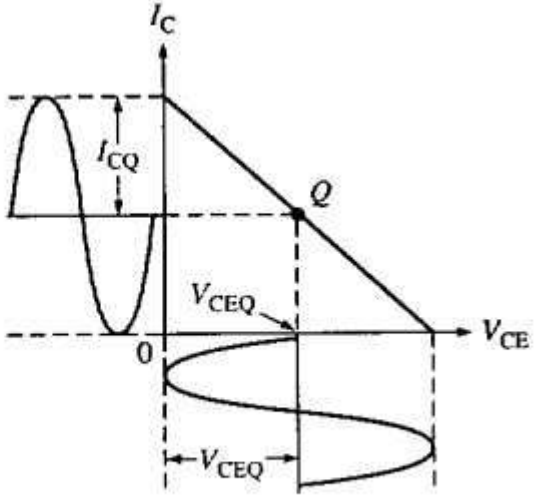
DC Biasing + AC signal



(a) Limited by saturation

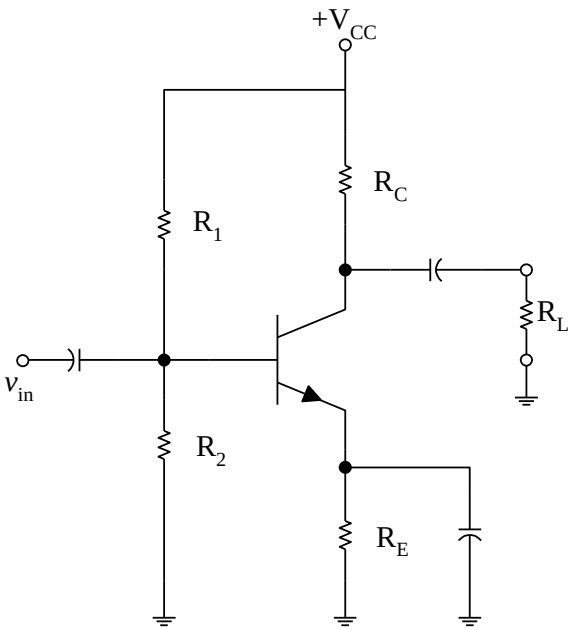


(b) Limited by cutoff

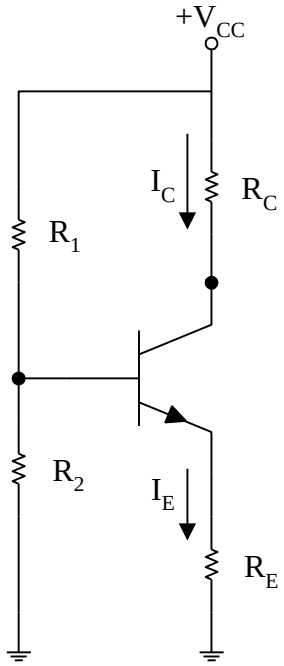


(c) Centered Q-point

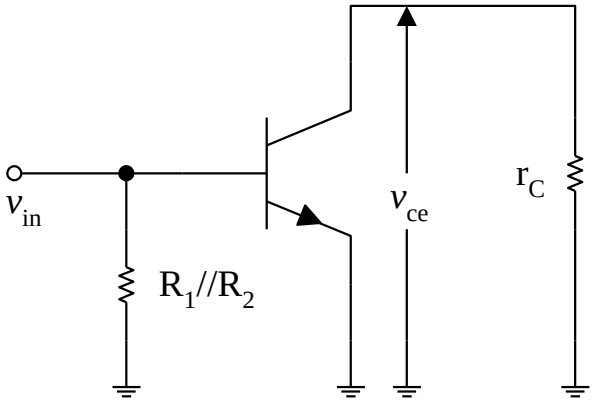
DC and AC Equivalent Circuits



Bias Circuit



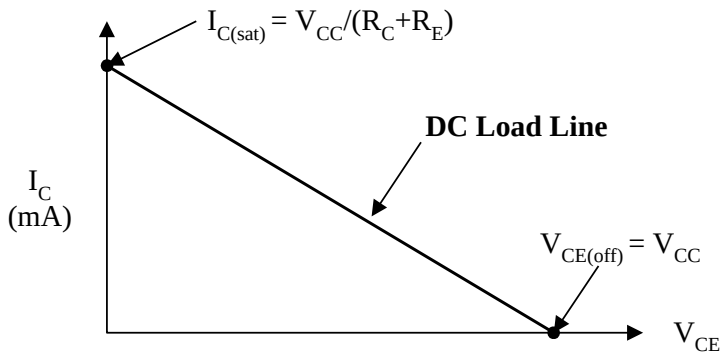
DC equivalent circuit



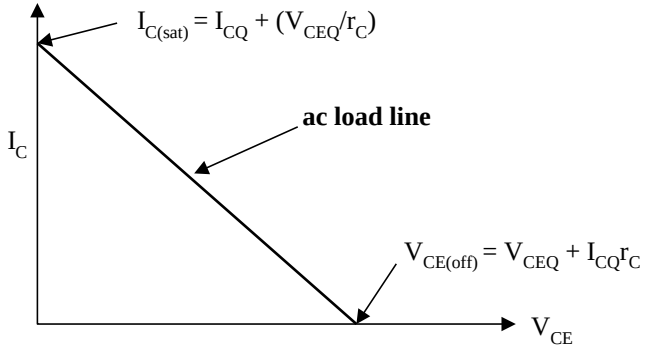
$r_C = R_C // R_L$

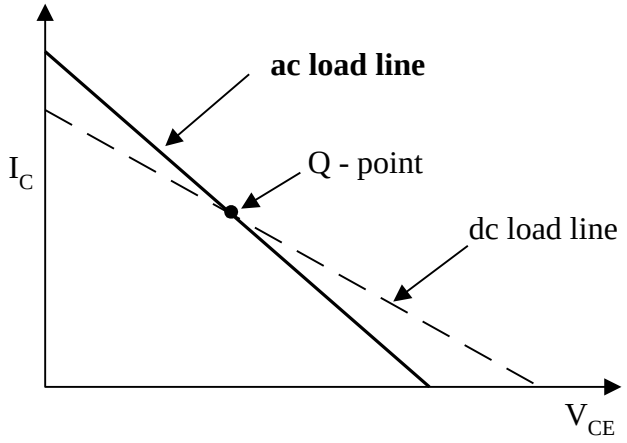
AC equivalent circuit

AC Load Line



- The ac load line of a given amplifier will **not follow** the plot of the dc load line.
- This is due to the dc load of an amplifier is different from the ac load.





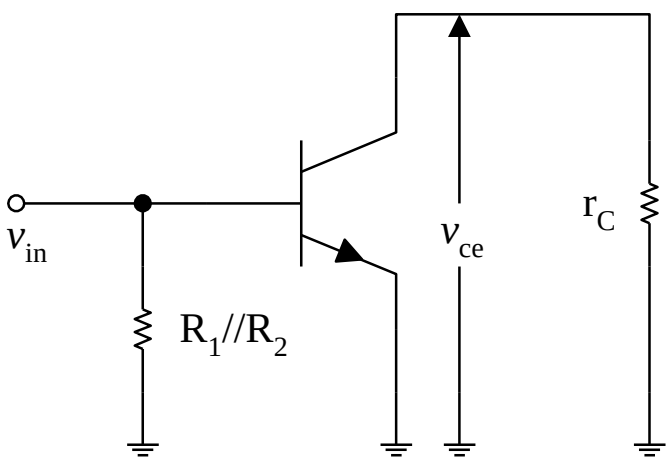
AC Load Line

What does the ac load line tell you?

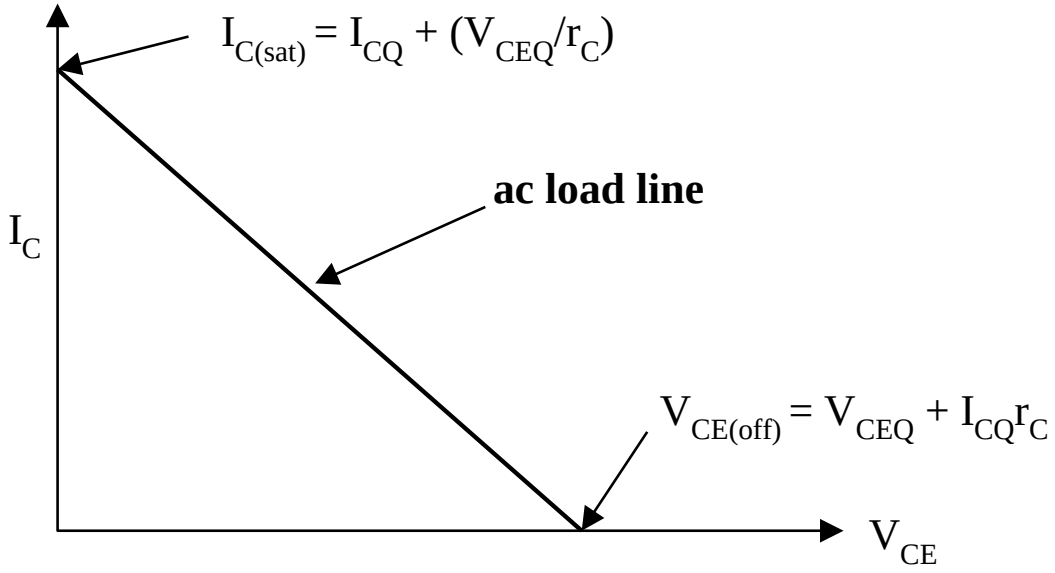
- The ac load line is used to tell you the maximum possible output voltage swing for a given common-emitter amplifier.
- In other words, the ac load line will tell you the maximum possible peak-to-peak output voltage (V_{pp}) from a given amplifier.
- This maximum V_{pp} is referred to as the **compliance** of the amplifier.

(AC Saturation Current $I_{c(sat)}$, AC Cutoff Voltage $V_{CE(off)}$)

AC Saturation Current and AC Cutoff Voltage



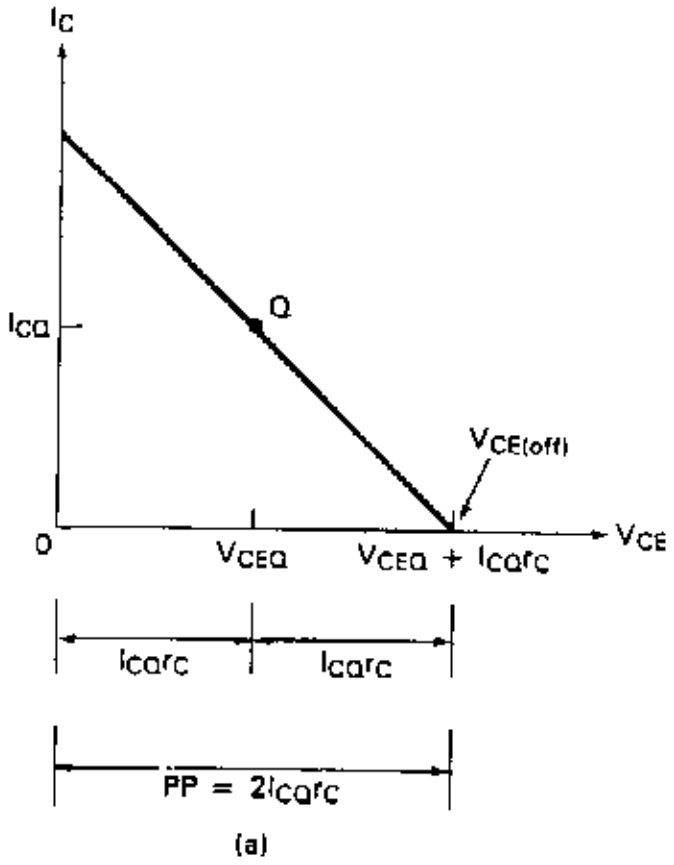
$r_C = R_C//R_L$

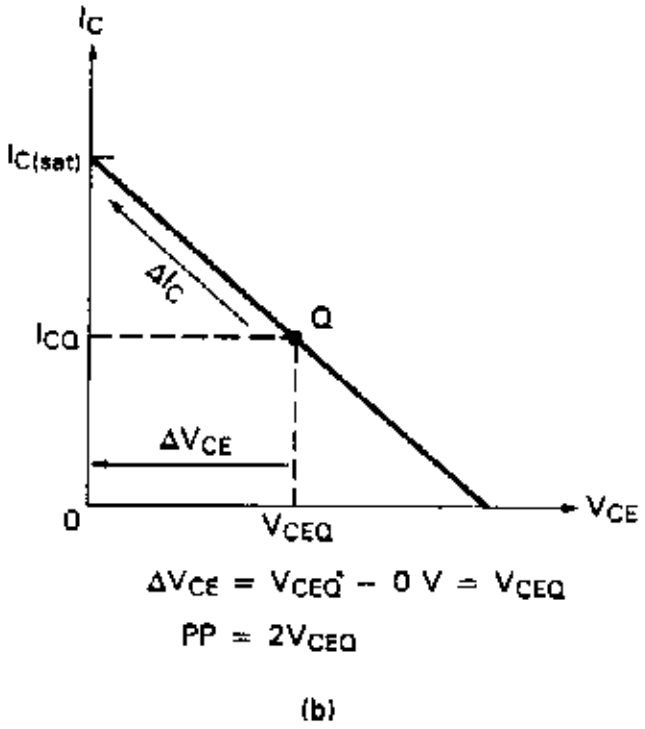


Amplifier Compliance

- The ac load line is used to tell the ***maximum possible output voltage swing for a given common-emitter amplifier***. In another words, the ac load line will tell the maximum possible peak-to-peak output voltage (V_{PP}) from a given amplifier. This maximum V_{PP} is referred to as the ***compliance*** of the amplifier.
- The compliance of an amplifier is found by determine the maximum possible of I_C and V_{CE} from their respective values of I_{CQ} and V_{CEQ}.

Maximum Possible Compliance





Compliance

The maximum possible transition for V_{CE} is equal to the difference between $V_{CE(off)}$ and V_{CEQ}. Since this transition is equal to $I_{CQ}r_C$, the maximum peak output voltage from the amplifier is equal to $I_{CQ}r_C$. Two times this value will give the maximum peak-to-peak transition of the output voltage:

$$\boxed{V_{PP} = 2I_{CQ}r_C} \qquad \text{(A)}$$

V_{PP} = the output compliance, in peak-to-peak voltage

I_{CQ} = the quiescent value of I_C

r_C = the ac load resistance in the circuit

Compliance

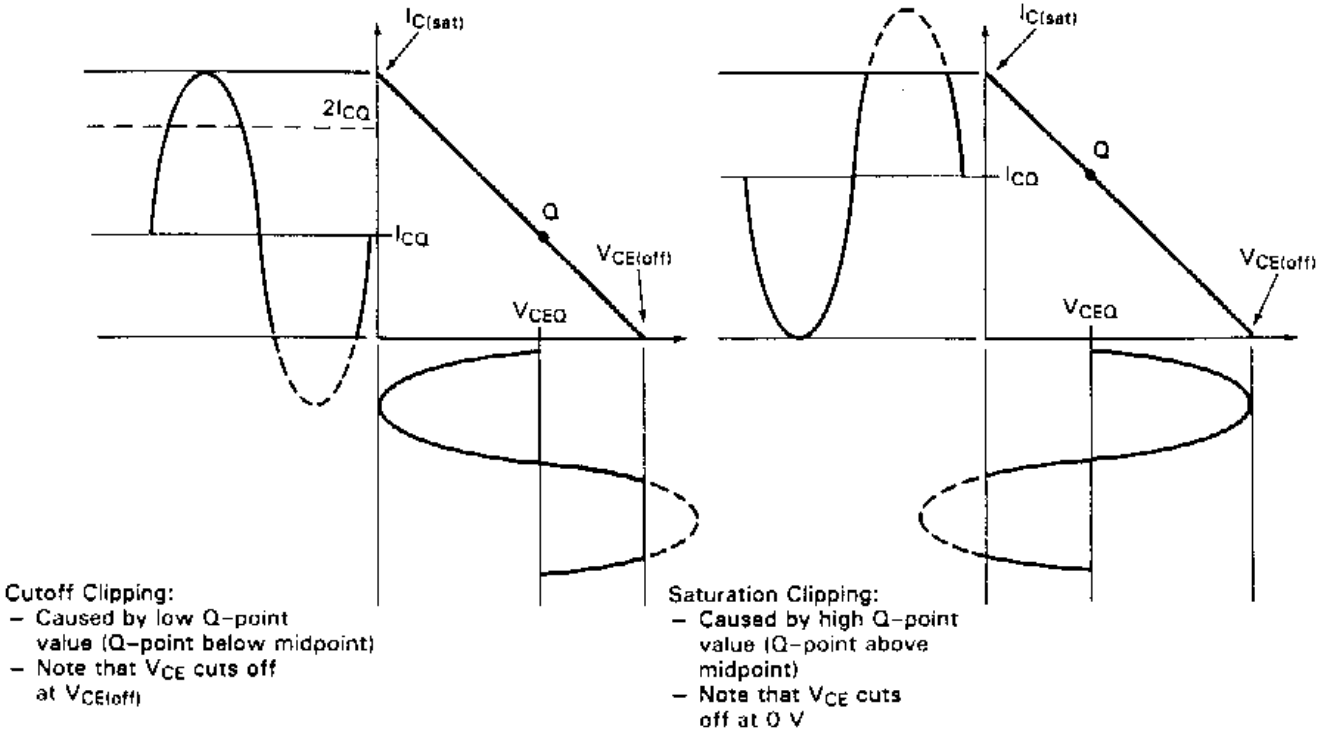
When $I_C = I_{C(sat)}$, V_{CE} is ideally equal to 0V. When $I_C = I_{CQ}$, V_{CE} is at V_{CEQ}. Note that when I_C makes its maximum possible transition (from I_{CQ} to $I_{C(sat)}$), the output voltage changes by an amount equal to V_{CEQ}. Thus the maximum peak-to-peak transition would be equal to twice this value:

$$V_{PP} = 2V_{CEQ} \qquad \text{(B)}$$

- Equation (A) sets the limit in terms of $V_{CE(off)}$. If the value obtained by this equation is exceed, the output voltage will try to exceed $V_{CE(off)}$, which is not possible. This is called cutoff clipping, because the output voltage is clipped off at the value of $V_{CE(off)}$.
- Equation (B) sets of the limit in terms of $I_{C(sat)}$. If the value obtained by this equation is exceed, the output will experience saturation clipping.

Cutoff and Saturation Clipping

- When determining the output compliance for a given amplifier, solve both equation (A) and (B). ***The lower of the two results is the compliance of the amplifier.***



Cutoff Clipping:
- Caused by low Q-point value (Q-point below midpoint)
- Note that V_{CE} cuts off at $V_{CE(off)}$

Saturation Clipping:
- Caused by high Q-point value (Q-point above midpoint)
- Note that V_{CE} cuts off at 0 V

Example

- For the voltage-divider bias amplifier shown in the figure, what is the ac and dc load line. Determine the maximum output compliance.